

A CACHE COHERENT SPLIT TRANSACTION MEMORY BUS
ARCHITECTURE AND PROTOCOL FOR A MULTI PROCESSOR CHIP
DEVICE

5 ABSTRACT OF THE DISCLOSURE

10 A cache coherent multiple processor integrated circuit. The circuit includes a plurality of processor units. The processor units are each provided with a cache unit. An embedded RAM unit is included for storing instructions and data for the processor units. A cache coherent bus is coupled to the processor units and the embedded RAM unit. The bus is configured to provide cache coherent snooping commands to enable the processor units to ensure cache coherency between their respective cache units and the embedded RAM unit. The multiple processor integrated circuit can further include an input output unit coupled to the bus to provide input and output transactions for the processor units. The bus is configured to provide split transactions for the processor units coupled to the bus, providing better bandwidth utilization of the bus. The bus can be configured to transfer an entire cache line for the cache units of the processor units in a single clock cycle, wherein the bus is 256 bits wide. The embedded RAM unit can be implemented as an embedded DRAM core. The multiple processor integrated circuit is configured to support a symmetric multiprocessing method for the plurality of processor units. The processor units can be configured to provide read data via the bus, as in a case of a read request by one processor when the read data is stored within a respective cache unit of another processor.

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